UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/870,458 | 06/01/2001 | Joshua M. Conner | 18153.0031 | 8446 |

23517 7590 03/25/2004

SWIDLER BERLIN SHEREFF FRIEDMAN, LLP
3000 K STREET, NW
BOX IP
WASHINGTON, DC 20007

| EXAMINER | |
|---|---|
| MEONSKE, TONIA L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | 6 |

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/870,458 | Applicant(s) CONNER ET AL. |
|---|---|---|
| | Examiner Tonia L Meonske | Art Unit 2183 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Oath/Declaration*

*1.* Applicant has not given a post office address anywhere in the application papers as required by 37 CFR 1.33(a), which was in effect at the time of filing of the oath or declaration. A statement over applicant's signature providing a complete post office address is required.

### *Specification*

*2.* The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 9-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 9 recites the limitation "the carry0 and carry 1 register" in line 6. There is insufficient antecedent basis for this limitation in the claim.

6. Claims 10-18 are rejected for incorporating the defects of claim 9.

*7.* Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Intel's Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual (herein after Intel).

10. Referring to claim 1, Intel has taught a method of processing a multi-precision shift instruction, comprising:

a. fetching and decoding a multi-precision shift instruction (page 18-7, First paragraph, Instructions are inherently fetched and decoded in every processing system. Pages 4-16 and 4-17, SHLD and SHRD);

b. executing the multi-precision shift instruction on an operand within a multi-word value to shift the operand and concatenate the shifted value with bits shifted out of a previous shift operation on the same multi-word value (Pages 4-16 and 4-17, SHLD and SHRD); and

c. outputting the result (page 4-16, The result is stored back into the destination operand.).

11. Referring to claim 2, Intel has taught the method according to claim 1, as described above, and further comprising storing the bits shifted out of the operand during the executing into a carry register (Pages 4-16 and 4-17, CF).

12. Referring to claim 3, Intel has taught the method according to claim 1, as described above, and wherein the multi-precision shift instruction is a shift left instruction (Page 4-16, SHLD).

13. Referring to claim 4, Intel has taught the method according to claim 1, as described above, and wherein the multi-precision shift instruction is a shift right instruction (Pages 4-16 and 4-17, SHRD).

14. Referring to claim 6, Intel has taught the method according to claim 1, as described above, and wherein the multi-precision shift instruction specifies a shift increment (Page 4-16, The CL register or an immediate byte in the instruction specifies the number of bits to be shifted.).

15. Referring to claim 7, Intel has taught the method according to claim 6, wherein the shift increment is greater than or equal to the number of bits in a word (Pages 4-19).

16. Referring to claim 8, Intel has taught the method according to claim 6, as described above, and wherein the shift increment is less than the number of bits in a word (Pages 4-16, 25-289 to 25-290).

***Claim Rejections - 35 USC § 103***

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 5 and 9-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel's Pentium Processor Family Developer's Manual, Volume 3: Architecture and Programming Manual (herein after Intel), in view of Silverbrook, US Patent 6,314,200.

19. Referring to claim 5, Intel has taught the method according to claim 1, as described above. Intel has not specifically taught wherein the concatenation step is performed by a logical OR operation. However, Silverbrook et al. have taught wherein the concatenation step is performed by a logical OR operation (column 222, lines 10-24) for the desirable purpose of implementing multiple precision shifting. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the concatenation step of Intel, include logical OR operation, as taught by Silverbrook et al., for the desirable purpose of implementing multiple precision shifting (column 222, lines 10-24).

20. Referring to claim 9, Intel has taught a processor for processing multi-precision shift instructions, comprising:

a. a program memory for storing instructions including a multi-precision shift instruction (Page 3-2, lines 1-3);

b. a program counter for identifying current instructions for processing (Page 3-15, section 3.3.5, Instruction Pointer); and

c. a barrel shifter for executing shift instructions (Page 4-16 and 4-17), the barrel shifter including:

d. a carry register for storing values shifted out of sections of the barrel shifter (Page 4-16 and 4-17, CF); and

e. logic for concatenating values stored in the carry 0 and carry 1 registers with values in the barrel shifter (pages 25-289 to 25-292), the barrel shifter executing a shift instruction fetched from the program memory to (page 18-7, First paragraph, Pages 4-16, 4-17, 25-289 to 25-292, Page 3-2, lines 1-3) a) load an operand into a section within the

barrel shifter (Pages 4-16, 4-17, 25-289 to 25-292), b) shift the operand (Pages 4-16, 4-17, 25-289 to 25-292), c) output the shifted value (Pages 4-16, 4-17, 25-289 to 25-292) and d) store into the carry register bits shifted out of the section of the barrel shifter (Pages 4-16, 4-17, 25-289 to 25-292).

21. Intel has not specifically taught all of the hardware logic required to implement the shift instructions. Intel has not specifically taught OR logic for concatenating values stored in the carry 0 and carry 1 registers with values in the barrel shifter. Silverbrook et al. have taught OR logic for concatenating values stored in the carry 0 and carry 1 registers with values in the barrel shifter (column 222, lines 10-24) in order to implement multiple precision shifting. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the invention of Intel, include the claimed OR logic, as taught by Silverbrook et al., for the desirable purpose of implementing multiple precision shifting (column 222, lines 10-24).

22. Referring to claim 10, Intel has taught the processor according to claim 9, as described above, and wherein the barrel shifter executes a multi-precision shift instruction to further e) concatenate the value in the carry register with the shifted operand prior to outputting the shifted value (pages 25-289 to 25-292).

23. Referring to claim 11, Intel has taught the processor according to claim 9, wherein the shift instruction is a shift left instruction (Pages 4-16, 4-17, 25-289 to 25-292, SHLD).

24. Referring to claim 12, Intel has taught the processor according to claim 9, as described above, and wherein the shift instruction is a shift right instruction (Pages 4-16, 4-17, 25-289 to 25-292, SHRD).

25. Referring to claim 13, Intel has taught the processor according to claim 9, as described above, and wherein the shift instruction is an arithmetic shift instruction (Pages 4-13 to 4-17).

26. Referring to claim 14, Intel has taught the processor according to claim 9, wherein the shift instruction is a logical shift instruction (Pages 4-13 to 4-17).

27. Referring to claim 15, Intel has taught the processor according to claim 9, as described above, and wherein the shift instruction specifies a shift increment (Pages 4-16 to 4-17).

28. Referring to claim 16, Intel has taught the processor according to claim 9, as described above, and wherein the barrel shifter executes at least two shift instructions to shift a multi-word value (Page 4-20, SHR, SHRD).

29. Referring to claim 17, Intel has taught the processor according 16, as described above, and wherein the first instruction of the at least two shift instructions is not a multi-precision shift instruction (Page 4-20, SHR).

30. Referring to claim 18, Intel has taught the processor according 16, as described above, and wherein the second and subsequent instructions of the at least two shift instructions is a multi-precision shift instruction (Page 4-20, SHRD).

***Conclusion***

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

RICHARD L. ELLIS
PRIMARY EXAMINER